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EXAMINER	
LU, TONY W	

ART UNIT	PAPER NUMBER
2878	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/680,179	SEKINE, HIROKAZU	
	Examiner	Art Unit	
	Tony Lu	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 08 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 03/01/2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 1,2,9,10 and 12 are objected to because of the following informalities:

As for claim 1, on line 11, the antecedent basis for "the floating region" is unclear.

As for claim 2, on line 4, the antecedent basis for "the facing sides" is unclear.

As for claim 9, on line 2, the antecedent basis for "the gate lines" is unclear.

As for claim 10, on line 2, the antecedent basis for "the gate lines" is unclear.

As for claim 12, on line 5 and page 33 on line 5, the antecedent bases for "the unit cell" and "the region" respectively are unclear.

Appropriate corrections and clarifications are required.

Claim Rejections - 35 USC § 112

Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claim 1, on lines 2-6, it is unclear on how many photodiodes are been claimed. Also note that there are multiple "a semiconductor substrate" in the claim, it is unclear on how many semiconductor substrates are been claimed.

As for claims 12, on lines, 2-6, it is unclear on how many photodiodes are been claimed. Also note that there are multiple instances of "a semiconductor substrate" in the claim, it is unclear on how many semiconductor substrates are been claimed.

Claims 2-11 are rejected as they depend on claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3,5-7,9,10,13,15 and 17, as understood by the examiner, are rejected under 35 U.S.C. 102(e) as being anticipated by Hashimoto US6956605.

With respect to claim 1, Hashimoto disclose an image pick up system comprising a plurality of unit cells being arranged in a matrix array on a semiconductor substrate(col.12), wherein each of the unit cells comprises a first and a second photodiodes(a11, a21 respectively) formed on the semiconductor substrate, a first readout transistor(MTX1) connected to the first photodiode and reading out signals thereof, a second readout transistor(MTX2) connected to the second photodiode and reading out signals thereof, a floating diffusion region(85) transmitting the signals and connected to the first and the second readout transistors, a reset transistor(MRES) connected to the floating diffusion region and resetting the potential of the region, an amplifying transistor(MSF) having a gate connected to the floating diffusion region and amplifying the signals, and a selecting transistor(MSEL) selectively addressing the amplifying transistor, the unit cell being connected to four address lines, comprising two

readout lines(108a, 108c) of the first and the second readout transistors, a reset line(112) of the reset transistor and a select line(110) of the selecting transistor, all of them extending in the horizontal direction, the unit cell being connected to a power line(91), and a signal line(87) connected to the amplifying transistor, both of them extending in the vertical direction of the matrix arrangement respectively, the address lines being superimposed in a double-layer every two lines and extended(as shown in figures.21-24, col.14), the first and the second photodiodes being located apart from each other with the first and the second readout transistors interposed between them, the floating diffusion region being approximately rectangular, and the first and the second readout transistors and the reset transistor being connected to respective sides of the floating diffusion region within the semiconductor substrate. The power line is inherently included in order to provide desired performances of the system.

With respect to claim 2, per the above discussion, Hashimoto discloses the first and the second readout transistors are connected to sides of the floating diffusion region facing thereto, and the reset transistor is connected to a side of the floating diffusion regions interposed between the sides connected by the first and the second readout transistors(see fig.22).

With respect to claim 3, per the above discussion, Hashimoto discloses the first and the second readout transistors are connected to neighboring sides of the floating diffusion region(see fig.22).

With respect to claim 5, per the above discussion, Hashimoto discloses the first and the second readout transistors, the floating diffusion region, the reset transistor, the

amplifying transistor and the selecting transistor are located in a region interposed by four gate lines extending respectively in the horizontal direction(see fig.2 and fig.21).

With respect to claim 6, per the above discussion, Hashimoto discloses the first and the second photodiodes are located facing to the vertical direction(see fig.1).

With respect to claim 7, per the above discussion, Hashimoto discloses the first and the second photodiodes are located facing to the vertical direction and offsetting to each other in the horizontal direction(see fig.1).

With respect to claim 9, per the above discussion, Hashimoto discloses one of the address lines of the double layer is the readout line of the first readout transistor and the reset line of the reset transistor.

With respect to claim 10, per the above discussion, Hashimoto discloses one of the address lines of the double layer is the readout line of the first readout transistor and the readout line of the second readout transistor.

With respect to claim 13, Hashimoto disclose an image pick up system comprising a plurality of unit cells being arranged in a matrix array on a semiconductor substrate(col.12), wherein each of the unit cells comprises a first and a second photodiodes(a11, a21 respectively) formed on the semiconductor substrate, a first readout transistor(MTX1) connected to the first photodiode and reading out signals thereof, a second readout transistor(MTX2) connected to the second photodiode and reading out signals thereof, a floating diffusion region(85) transmitting the signals and connected to the first and the second readout transistors, a reset transistor(MRES) connected to the floating diffusion region and resetting the potential of the region, an

amplifying transistor(MSF) having a gate connected to the floating diffusion region and amplifying the signals, and a selecting transistor(MSEL) selectively addressing the amplifying transistor, the unit cell being connected to four gate lines, comprising two readout lines(108a, 108c) of the first and the second readout transistors, a reset line(112) of the reset transistor and a select line(110) of the selecting transistor, all of them extending in the horizontal direction, the gate lines being superimposed in a double-layer every two lines and extended(as shown in figures.21-24, col.14), the first and the second photodiodes being located apart from each other in vertical direction with the first and the second readout transistors interposed between them, the floating diffusion region being approximately rectangular, the first and the second readout transistor sharing a floating diffusion region to become a drain and being located between the first and the second photodiodes, and the reset transistor being provided directly adjacent to the floating diffusion region(see fig.1 and fig.21-22).

With respect to claim 15, Hashimoto disclose an image pick up system comprising a plurality of unit cells being arranged in a matrix array on a semiconductor substrate(col.12), wherein each of the unit cells comprises a first and a second photodiodes(a11, a21 respectively) formed on the semiconductor substrate, a first readout transistor(MTX1) connected to the first photodiode and reading out signals thereof, a second readout transistor(MTX2) connected to the second photodiode and reading out signals thereof, a floating diffusion region(85) transmitting the signals and connected to the first and the second readout transistors, a reset transistor(MRES) connected to the floating diffusion region and resetting the potential of the region, an

amplifying transistor(MSF) having a gate connected to the floating diffusion region and amplifying the signals, and a selecting transistor(MSEL) selectively addressing the amplifying transistor, the unit cell being connected to four gate lines, comprising two readout lines(108a, 108c) of the first and the second readout transistors, a reset line(112) of the reset transistor and a select line(110) of the selecting transistor, all of them extending in the horizontal direction, the gate lines being superimposed in a double-layer every two lines and extended(as shown in figures.21-24, col.14), the first and the second photodiodes being located apart from each other in vertical direction with the first and the second readout transistors interposed between them, the floating diffusion region being approximately rectangular, the first and the second readout transistor sharing a floating diffusion region to become a drain and being located between the first and the second photodiodes, wherein the amplifying transistor, the reset transistor, and the selecting transistor being all formed in a region interposed by the readout lines of the first and the second readout transistor(see fig.1), and the reset transistor being provided directly adjacent to the floating diffusion region(see fig.1 and fig.21-22).

With respect to claim 17, per the above discussion, Hashimoto discloses the centers of the first and second photodiodes are horizontally offset to each other.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 8,11,12,14 and 16, as understood by the examiner, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto US6956605.

With respect to claim 4, per the above discussion, although Hashimoto lacks a clear teaching of the floating diffusion region is constituted to be one of electrodes of the first readout transistor, the second readout transistor and the reset transistor, which is common thereto, it would have been inherently included as a somewhat standard form of a semiconductor photosensing structure, however, if not, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hashimoto accordingly in order to provide a more specific formation of the pixel cell structure.

With respect to claim 8, per the above discussion, although Hashimoto fails to specify a detailed interconnection between the diffusion region, the readout transistors, the reset transistor and the amplify transistor as claimed, selecting a particular wiring/contacting connection between elements/components in an optical system in order to provide a more compact design for the system would have been obvious to one of ordinary skill in the art. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hashimoto accordingly in order to provide a better circuitry design for the image cell of the system.

With respect to claim 11, per the above discussion, although Hashimoto lacks a clear teaching of the four address lines extending in the horizontal direction are formed by polycrystalline silicon and the two lines extending in the vertical direction are metal,

selecting a specific type of material for forming components of the system in order to provide durable and/or better performance components would have been obvious to one of ordinary skill in the art.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hashimoto accordingly in order to provide long lasting and/or cost-effective components for the system.

With respect to claim 12, Hashimoto disclose an image pick up system comprising a plurality of unit cells being arranged in a matrix array on a semiconductor substrate(col.12), wherein each of the unit cells comprises a first and a second photodiodes(a11, a21 respectively) formed on the semiconductor substrate, a first readout transistor(MTX1) connected to the first photodiode and reading out signals thereof, a second readout transistor(MTX2) connected to the second photodiode and reading out signals thereof, a floating diffusion region(85) transmitting the signals and connected to the first and the second readout transistors, a reset transistor(MRES) connected to the floating diffusion region and resetting the potential of the region, an amplifying transistor(MSF) having a gate connected to the floating diffusion region and amplifying the signals, and a selecting transistor(MSEL) selectively addressing the amplifying transistor, the unit cell being connected to four address lines, comprising two readout lines(108a, 108c) of the first and the second readout transistors, a reset line(112) of the reset transistor and a select line(110) of the selecting transistor, all of them extending in the horizontal direction, the unit cell being connected to a power line(91), and a signal line(87) connected to the amplifying transistor, both of them

extending in the vertical direction of the matrix arrangement respectively, the address lines being superimposed in a double-layer every two lines and extended(as shown in figures.21-24, col.14), the first and the second photodiodes being located apart from each other with the first and the second readout transistors interposed between them, the floating diffusion region being approximately rectangular, and the first and the second readout transistors and the reset transistor being connected to respective sides of the floating diffusion region within the semiconductor substrate.

Although Hashimoto lacks a clear teaching of the power line is connected to specific terminals of the reset transistor, selecting transistor and amplifying transistor, it would have been inherently included for supplying sufficient voltage/current/power to the transistors, however, if not, It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hashimoto accordingly in order to provide a more compact wiring connection for the transistor of the system.

Hashimoto further lacks a clear teaching of a metal line for connecting the amplifying transistor and the floating diffusion region. The use of a metal line for transmitting voltage/signal/current would have been obvious to one of ordinary skill in the art. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hashimoto accordingly in order to provide proper means for connecting components of the system.

With respect to claim 14, per the above discussion, although Hashimoto fails to specify a detailed interconnection between the diffusion region, the readout transistors, the reset transistor and the amplify transistor as claimed, selecting a particular

wiring/contacting connection between elements/components in an optical system in order to provide a more compact design for the system would have been obvious to one of ordinary skill in the art. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hashimoto accordingly in order to provide a better circuitry design for the image cell of the system. The further citation regarding to a line being pulled out from the floating diffusion region to the gate of the amplifying transistor would have been obvious for providing/establishing a proper connecting means between the components of the system.

With respect to claim 16, per the above discussion, although Hashimoto fails to specify a detailed interconnection between the floating diffusion region and the readout transistors as claimed, selecting a particular wiring/contacting connection between elements/components in an optical system in order to provide a more compact design for the system would have been obvious to one of ordinary skill in the art. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hashimoto accordingly in order to provide a better circuitry design for the image cell of the system.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1) Loose US6759641 discloses an imager system with adjustable resolution having a power line(v+) extended in vertical direction connected to the reset transistor and the select transistor.

2) Guidash US6107655 discloses an active pixel sensor with shared amplifier readout(fig.2b).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tony Lu whose telephone number is 5712728448. The examiner can normally be reached on M-F 9:00am- 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on 5712722328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TL

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